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KATTEN MUCHIN ROSENMAN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,553	NODA ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/27/06, 7/30/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 and 14 have been examined.

2. Acknowledgement of papers filed: oath/declaration, specification, drawings, claims on 27 July 2006.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claim 2 is objected to because of the following informalities: "the second processor further comprises an address notification unit which notifies communicates the return" does not appear to be grammatically correct. Please consider revising. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki (U.S. Patent No. 6,807,620) in view of Dye (U.S. Patent No. 5,706,478) in further view of Cilvin (U.S. Patent No. 6,671,196).

7. Regarding Claim 1, Suzuoki discloses a multiprocessor system comprising a first processor (Fig. 1 reference 5) and a second processor (Fig. 1 reference 3). The remaining limitations are best shown after the combination.

Suzuoki fails to disclose situations in which the graphics processor has a subroutine call and return.

Dye discloses the limitations that Suzuoki lacks (col 13 line 47 to col 14 line 5)

Suzuoki would have been motivated to allow a subroutine call from the graphics processor with a return address in order to improve the flexibility of the graphics processor program execution.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Suzuoki and incorporate the subroutine call and return of the graphics progress of Dye.

Suzuoki and Dye fail to disclose what occurs when the local stacks of the graphics processor becomes full.

Cilvin discloses the limitations Suzuoki/Dye lacks (col 5 lines 22-40)

Suzuoki/Dye would have been motivated to copy a full stack to a primary memory to improve the amount of nested subroutine calls (and other data stores) that are available to the graphics processor.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Suzuoki/Dye and allow a full stack of the graphics processor subroutine calls to be saved to the primary memory (Suzuoki fig. 1 reference 7). The combination would be as follows: the first processor (fig. 1 reference 5) comprises an interrupt generation unit which generates an interrupt to the second processor (Cilvin col 5 lines 22-40 – the command to save information in the main memory via the main processor is interpreted to be an interrupt) when the first processor executes a predetermined call instruction in a running main routine (Dye col 14 line 47 to col 14 line 5); and the second processor comprises an address save unit (In particular, the unit that completes Cilvin col 5 lines 22-40 within Suzuoki Fig. 1 reference 7 via Fig. 1 reference 3) which saves a return address for returning to the main routine upon completion of processing of a subroutine called by the call instruction to a predetermined memory area when the second processor receives an interrupt from the interrupt generation unit (Dye col 5 lines 22-40).

8. Regarding Claim 2, Suzuoki/Dye/Cilvin discloses the multiprocessor system according to claim 1, wherein: the interrupt generation unit generates an interrupt to the second processor again when a predetermined return instruction is executed in the subroutine; and the second processor further comprises an address notification unit which notifies communicates the return address to the first processor when receiving the re-generated interrupt (Cilvin col 5 lines 22-40).

9. Regarding Claim 3, Suzuoki/Dye/Cilvin discloses the multiprocessor system according to claim 1, wherein the first processor comprises a fetcher (Suzuoki Fig. 7 reference 151) which fetches an instruction (Suzuoki col 4 lines 58 to 65); and the return address is set as a target address to be accessed by the fetcher (Dye col 13 lines 47 to col 14 line 5).

10. Regarding Claim 4, Suzuoki/Dye/Cilvin discloses a multiprocessor system comprising a first processor (Suzuoki Fig. 1 reference 5) and a second processor (Suzuoki Fig. 1 reference 3), wherein: the first processor comprises an interrupt generation unit which generates an interrupt to the second processor when the first processor executes a predetermined call instruction or jump instruction (Cilvin col 5 lines 22-40); and the second processor comprises: an address extraction unit which extracts a call destination address or jump destination address stored dividedly in formats of the call instruction or the jump instruction (Dye col 13 line 47 to col 14 line 5) and an accompanying execution stop instruction when the second processor receives the interrupt from the first processor (Dye col 13 line 47 to col 14 line 5); and an address notification unit which communicates the acquired call destination address or jump destination address to the first processor (Dye col 13 line 47 to col 14 line 5).

11. Regarding Claim 5, Suzuoki/Dye/Cilvin discloses the multiprocessor system according to claim 4, wherein the first processor comprises a fetcher (Suzuoki Fig. 7 reference 151) which fetches an instruction (Suzuoki col 4 lines 58 to 65); and the call

destination address or the jump destination address is set as a target address to be accessed by the fetcher (Dye col 13 lines 47 to col 14 line 5).

12. Regarding Claim 6, Suzuoki/Dye/Cilvin discloses a multiprocessor system comprising a graphics processor (Suzuoki Fig. 1 reference 5) and a main processor (Suzuoki Fig. 1 reference 3), wherein the graphics processor comprises: a direct memory access controller (DMAC) which reads instructions written in a display list from a memory sequentially (Dye col 13 line 47 to col 14 line 5); a decoder which decodes the read instructions sequentially; and an interrupt generation unit which generates a shift interrupt to the main processor when a decoded instruction is a predetermined call instruction included in a main routine of the display list and generates a return interrupt to the main processor when a decoded instruction is a return instruction included in a subroutine called by the call instruction (Cilvin col 5 lines 22-40), the main processor comprises: an address save unit which saves a return address for returning to the main routine upon completion of processing of the subroutine to a predetermined memory when the main processor receives the shift interrupt from the interrupt generation unit (Cilvin col 5 lines 22-40); and an address notification unit which reads the return address from the predetermined memory and communicates the return address to the graphics processor when the main processor receives the return interrupt from the interrupt generation unit (Cilvin col 5 lines 22-40), and the return address communicated to the graphics processor is set as a target address to be accessed by the DMAC (Dye col 13 line 47 to col 14 line 5).

13. Regarding Claim 7, Suzuoki/Dye/Cilvin discloses a multiprocessor system comprising a graphics processor (Suzuoki fig 1 reference 5) and a main processor (Suzuoki fig. 1 reference 3), wherein the graphics processor comprises: a direct memory access controller (DMAC) which reads instructions written in a display list from a memory sequentially (Dye col 13 line 47 to col 14 line 5); a decoder which decodes the read instructions sequentially; and an interrupt generation unit which generates an interrupt to the main processor when a decoded instruction is a predetermined call instruction or a jump instruction included in the display list (Cilvin col 5 lines 22-40), the main processor comprises an address notification unit which acquires a call destination address or a jump destination address stored dividedly in formats of the call instruction or the jump instruction and an accompanying execution stop instruction (Cilvin col 5 lines 22-40), and communicates the call destination address or the jump destination address to the graphics processor when the main processor receives the interrupt from the interrupt generation unit (Cilvin col 5 lines 22-40), and the call destination address or the jump destination address communicated to the graphics processor is set as a target address to be accessed by the DMAC (Dye col 13 line 47 to col 14 line 5).

14. Regarding Claim 8, Suzuoki/Dye/Cilvin discloses a method of executing a program in a multiprocessor system, the method comprising, executing a call instruction in a main routine running by a first processor (Dye col 13 line 47 to col 14 line 5), delegating to a second processor the task of saving a return address for returning to the

main routine upon completion of processing of a subroutine called by the call instruction (Cilvin col 5 lines 22-40).

15. Regarding Claim 9, Suzuoki/Dye/Cilvin discloses the method of executing a program in a multiprocessor system according to claim 8, wherein: if a stack area inside the first processor has a free space, the first processor saves the return address to the stack area by itself; and if the stack area has no free space, the save of the return address is delegated to the second processor (Cilvin col 5 lines 22-40).

16. Regarding Claim 10, Suzuoki/Dye/Cilvin discloses the method of executing a program in a multiprocessor system according to claim 8, wherein: if the call instruction does not explicitly instruct to delegate the task of saving the return address to the second processor, the first processor saves the return address to a stack area built in itself; and if the call instruction explicitly instructs to delegate the task of saving the return address to the second processor, the first processor delegates the task of saving the return address to the second processor (Cilvin col 5 lines 22-40).

17. Regarding Claim 11, Suzuoki/Dye/Cilvin discloses a method of executing a program in a multiprocessor system, the method comprising, executing a call instruction or a jump instruction by a first processor, delegating a task of acquiring a full address of a call destination address or a jump destination address to a second processor (Cilvin col 5 lines 22-40).

18. Regarding Claim 12, Suzuoki/Dye/Cilvin discloses a method of executing a program in a multiprocessor system according to claim 11, wherein delegating a task of acquiring the full address of the call destination address or the jump destination address to a second processor, if the number of bits of the call destination address or the jump destination address exceeds the number of bits acquirable by the first processor (Cilvin col 5 lines 22-40).

19. Regarding Claim 14, Suzuoki/Dye/Cilvin discloses a method of executing a program in a multiprocessor system according to claim 11, wherein delegating the task of acquiring the full address of the call destination address or the jump destination address to a second processor if the call instruction or the jump instruction explicitly instructs to delegate the task of acquiring the call destination address or the jump destination address to the second processor (Cilvin col 5 lines 22-40).

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRIAN P. JOHNSON whose telephone number is (571)272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian Johnson/ Patent Examiner, Art Unit 2183

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183